IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Title:	SEMICONDUCTOR PACKAGE AND METHOD FOR FABRICATING THE SAME		
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CERTIFICATE OF TRANSLATION OF FOREIGN PRIORITY DOCUMENT UNDER 37 C.F.R. § 1.55(a)

Attached hereto as Exhibit A is an English language translation of Korean Patent Application 1999-37928, which was filed in Korea on September 7, 1999. I, the undersigned, hereby certify that the English language translation attached as Exhibit A is an accurate translation of Korean patent Application 1999-37928.

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1999-37928

TITLE: SEMICONDUCTOR PACKAGE SUBSTRATE AND METHOD FOR MANUFACTURING SEMICONDUCTOR PACKAGES USING THE SAME

[ABSTRACT]

Disclosed is a semiconductor package substrate capable of minimizing warpage during a wire bonding or molding process by forming a cutting line on integral coverlay tape, which is attached to the substrate during manufacturing processes and which can be removed easily, and a method for manufacturing semiconductor packages using the same. The semiconductor package substrate includes a resin layer having a number of sub-strips connected to one another to constitute a main-strip while slots extend a predetermined length and act as boundaries among the sub-strips, each sub-strip having a number of through-holes grouped in predetermined rows and columns while being spaced a predetermined distance from one another so that a semiconductor chip can be positioned thereon; a conductive circuit pattern having bond fingers and ball lands formed on a surface of the resin layer along an outer peripheral edge of the through-holes of the sub-strips so that semiconductor chips can be connected to the bond fingers by connection means and conductive balls can be melted and attached to the ball lands; a cover coat formed on a surface of the resin layer and the circuit pattern while exposing the bond fingers and the ball

lands; and integral coverlay tape attached to a surface of the resin layer constituting the main strip to close the through-holes, the coverlay tape having a cutting line at an interface between two sub-strips.

[REPRESENTATIVE FIGURE]

FIG. 1b

[SPECIFICATION]

[BRIEF DESCRIPTION OF THE DRAWINGS]

FIG. 1a is a top view showing a semiconductor package substrate according to the present invention;

FIG. 1b is a bottom view showing a semiconductor package substrate according to the present invention, which has tape attached thereto;

FIGs. 2a to 2h show a series of steps of a method for manufacturing semiconductor packages according to the present invention, respectively; and

FIG. 3 is a sectional view showing a conventional ultra-slim semiconductor package.

[BRIEF DESCRIPTION OF REFERENCE NUMERALS]

100: substrate

2: sub-strip

4: main-strip

6: resin layer

8: through-hole

12: bond finger

14: ball land

16: cover coat

18: ground ring

22: ground plane

26: slot

28: index hole

30: coverlay tape

32: cutting line

34: punch

200: semiconductor package

42: semiconductor chip

44: connection means

46: sealant

48: conductive ball

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[RELATED FIELD OF THE INVENTION AND PRIOR ART]

The present invention relates to a semiconductor package substrate and a method for manufacturing semiconductor packages

using the same. More particularly, the present invention relates to a semiconductor package substrate capable of minimizing warpage during a wire bonding or molding process by forming a cutting line on integral coverlay tape, which is attached to the substrate, and a method for manufacturing semiconductor packages using the same.

According to current trends towards lightness, slimness, and compactness of semiconductor chips, as well as compactness of various electronic devices, semiconductor packages, which support semiconductor chips on motherboards and mediate input/output signals, have been manufactured in an ultra-slim type or in a chip size.

FIG. 3 shows a conventional ultra-slim semiconductor package 200', the structure of which will now be described briefly with reference to the drawing.

As shown, a substrate 100' includes a semiconductor chip 42', which has an input/output pad formed on a surface thereof. The substrate 100' has a through-hole 8' formed along the outer peripheral edge of the semiconductor chip 42' to position it thereon. The substrate 100' has a resin layer 6', as a basic layer, and a circuit pattern, including a number of bond fingers 12' and ball lands 14', formed on a surface of the resin layer 6'. The surface of the resin layer 6' and the circuit pattern is coated with a cover coat 16' while exposing

the bond fingers 12′ and the ball lands 14′. The input/output pad of the semiconductor chip 42′ is electrically connected to the bond fingers 12′ of the substrate 100′ by electrical connection means 44′, such as conductive wires. The semiconductor chip 42′, which is positioned within the through-hole 8′ of the substrate 100′, the connection means 44′, and a part of the substrate 100′ are enclosed with a sealant 46′ while exposing a surface of the semiconductor chip 42′ to the exterior of the sealant 46′. A number of conductive balls 48′ are melted and attached to the ball lands 14′ of the substrate 100′ to be mounted on a motherboard later.

A method for manufacturing semiconductor packages, constructed as above, will now be described briefly.

A substrate is provided, which has a resin layer as a basic layer and a number of bond fingers and ball lands formed on a surface of the resin layer. The substrate is coated with a cover coat while exposing the bond fingers and the ball lands. The substrate has a through-hole formed at the center thereof. The substrate normally has a number of units formed within a single unit to obtain separate semiconductor packages.

A semiconductor chip, which has a number of input/output pads on a surface thereof, is positioned within the through-hole of the substrate. Coverlay tape (not shown) is attached

to a surface of the substrate to close the through-hole, and the semiconductor chip is attached to the coverlay tape.

The input/output pads of the semiconductor chip are electrically connected to the bond fingers of the substrate by electrical connection means.

Predetermined regions of the semiconductor chip within the through-hole, the connection means, and the substrate are molded with a sealant.

A number of conductive balls are melted and attached to the ball lands, which are formed on the substrate, to form final input/output terminals. Then, the coverlay tape is removed from the substrate.

Finally, the strip-shaped substrate is subjected to singulation to obtain separate semiconductor packages, which correspond to the respective units.

Meanwhile, when such a substrate is manufactured, integral coverlay tape is attached to a surface of the substrate so that semiconductor chips can be molded. The coverlay tape has a different thermal expansion coefficient from that of the substrate and causes various problems.

In particular, the difference in thermal expansion coefficient between the substrate and the coverlay tape causes warpage of the substrate during a wire bonding or molding process, which requires a high temperature condition. This

results in poor wire bonding and molding and seriously degrades the reliability of semiconductor packages.

In addition, semiconductor chips of conventional ultra-slim semiconductor packages may accumulate static electricity during a molding process. If the static electricity is abruptly discharged, it may damage the semiconductor chips or cause circuit patterns of the substrate to short-circuit. This problem must be solved rapidly.

When semiconductor packages are manufactured, as mentioned above, coverlay tape must be attached to and removed from the substrate. The coverlay tape tends to be attached to an entire surface of the substrate and is not easily removed. If an excessive force is applied to remove the coverlay tape, the substrate may be damaged.

[TECHNICAL OBJECT TO ACHIEVE]

Accordingly, the present invention has been made to solve the above-mentioned problems occurring in the prior art, and an object of the present invention is to provide a semiconductor package substrate capable of minimizing warpage during a wire bonding or molding process by forming a cutting line on integral coverlay tape, which is attached to the substrate during manufacturing processes and which can be removed easily,

and a method for manufacturing semiconductor packages using the same.

[CONSTRUCTION AND OPERATION OF THE INVENTION]

In order to accomplish this object, there is provided a semiconductor package substrate including a resin layer having a number of sub-strips connected to one another to constitute a main-strip while slots extend a predetermined length and act as boundaries among the sub-strips, each sub-strip having a number of through-holes grouped in predetermined rows and columns while being spaced a predetermined distance from one another so that a semiconductor chip can be positioned thereon; a conductive circuit pattern having bond fingers and ball lands formed on a surface of the resin layer along an outer peripheral edge of the through-holes of the sub-strips so that semiconductor chips can be connected to the bond fingers by connection means and conductive balls can be melted and attached to the ball lands; a cover coat formed on a surface of the resin layer and the circuit pattern while exposing the bond fingers and the ball lands; and integral coverlay tape attached to a surface of the resin layer constituting the main strip to close the through-holes, the coverlay tape having a cutting line at an interface between two sub-strips.

The cutting line of the coverlay tape may span an entire width of the coverlay tape, or spans a portion of an entire width of the coverlay tape including a region on the slot.

In accordance with another aspect of the present invention, there is provided a method for manufacturing semiconductor packages including the steps of providing a semiconductor package substrate including a resin layer having a number of sub-strips connected to one another to constitute a main-strip while slots extend a predetermined length and act as boundaries among the sub-strips, each sub-strip having a number of through-holes grouped in predetermined rows and columns while being spaced a predetermined distance from one another so that a semiconductor chip can be positioned thereon, a conductive circuit pattern having bond fingers and ball lands formed on a surface of the resin layer along an outer peripheral edge of the through-holes of the sub-strips so that semiconductor chips can be connected to the bond fingers by connection means and conductive balls can be melted and attached to the ball lands, and a cover coat formed on a surface of the resin layer and the circuit pattern while exposing the bond fingers and the ball lands; attaching integral coverlay tape to a surface of each sub-strip of the substrate to cover each through-hole of the sub-strip, the coverlay tape having a cutting line at an interface between two

sub-strips; positioning semiconductor chips in the respective through-holes and attaching the semiconductor chips to the coverlay tape; connecting the semiconductor chips to the bond fingers on the outer peripheral edge of the through-holes with electrical connection means; filling the through-holes with a sealant to protect the semiconductor chips and the connection means from external environments; removing the coverlay tape from the substrate; melting and attaching conductive balls to the ball lands on the outer peripheral edge of the through-holes; and cutting the outer peripheral edge of the through-holes to obtain separate semiconductor packages in a singulation process.

In the step of attaching integral coverlay tape, the cutting line of the coverlay tape may span an entire width of the coverlay tape, or span a portion of an entire width of the coverlay tape including a region on the slot.

The semiconductor package substrate and method for manufacturing semiconductor packages using the same according to the present invention are advantageous in that a cutting line is formed on the integral coverlay tape, which is attached to the substrate, to minimize warpage of the substrate resulting from the difference in thermal expansion coefficient, which increases in proportion to the length, and to prevent

defects from occurring during processes for manufacturing semiconductor packages.

A preferred embodiment of the present invention will now be described in detail with reference to the accompanying drawings.

FIGs. 1a and 1b are top and bottom views showing a substrate 100 for semiconductor packages 200 according to the present invention, respectively.

A resin layer 6 is provided in an approximately rectangular shape as a basic material. A sub-strip 2 has a number of through-holes 8 grouped in a number of rows and columns (i.e. in a matrix shape) while being spaced a predetermined distance from one another, so that a semiconductor chip (not shown) can be positioned thereon. A number of sub-strips 2 are connected to one another in the transverse direction and constitute a main-strip 4 in such a manner that their slots 26, which extend a predetermined distance in the longitudinal direction, act as borders between them.

Each sub-strip 2 has bond fingers 12 formed on a surface of the resin layer 6 along the outer peripheral edge of the through-holes 8, in order to be to a semiconductor chip 42 by electrical connection means 44 (e.g. gold wires or aluminum wires), and ball lands 14 connected to the bond fingers 12 so

that conductive balls 48 (e.g. solder balls) can be melted and attached thereto later. The bond fingers 12 and the ball lands 14 are defined as conductive circuit patterns.

The surface of the resin layer 6 and the circuit patterns is coated with a cover coat 16 using a high-molecular resin while exposing the bond fingers 12 and the ball lands 14 to the exterior. The cover coat 16 protects the circuit patterns from external environments and secures the overall rigidity of the substrate 100.

The resin layer 6 has conductive ground planes 22 formed on a surface thereof near the periphery of the substrate 100 with a predetermined area. The ground planes 22 are exposed by the cover coat and are electrically connected to the ground rings 18. The ground planes 22 may be formed on both surfaces of the resin layer 6, in contrast to the ground rings 18, to facilitate discharge of static elasticity, which may occur during manufacturing processes, to the exterior.

As shown in FIG. 1b, the coverlay tape 30 has the same size as the main-strip 4 to be attached to an entire surface of the main-strip 4. When attached to the main-strip 4, the integral coverlay tape 30 has a cutting line 32 formed at an interface between two sub-strips 2.

In general, the amount of deformation resulting from the difference in thermal expansion coefficient between the

substrate and the coverlay tape during a wire bonding or molding process, which requires a high temperature condition, is given as follows:

$$\Delta L = L \times \alpha$$

wherein, ΔL is the amount of deformation, L is the length of the tape, and α is modulus of deformation.

Therefore, according to the present invention, the length of the tape is reduced as much as the length the cutting line formed on the coverlay tape. As a result, the thermal expansion coefficient, which increases in proportion to the length, can decrease.

Preferably, the cutting line 32 of the coverlay tape is formed on the slot 26 at the interface between two sub-strips 2. In addition, the width of the cutting line 32 (in the transverse direction of the drawing) is preferably smaller than the width of the slot (in the transverse direction of the drawing), so that the coverlay tape 30 can be easily removed in processes for manufacturing semiconductor packages 200 (described later), but the size is not limited to that in the present invention.

The cutting line 32 may span an entire width of the coverlay tape 30 (in the longitudinal direction of the drawing). Alternatively, the cutting line 32 may span a portion of the entire width of the coverlay tape, including the

slot 26, but the size is not limited to that in the present invention.

Reference numeral 28 refers to an index hole for loading and retaining the substrate 100 on various manufacturing equipment.

As mentioned above, the substrate 100 for semiconductor packages 200 according to the present invention has a cutting line 32 formed on the integral coverlay tape, which is attached to the substrate 100, to minimize warpage resulting from the difference in thermal expansion coefficient, which increases in proportion to the length.

In addition, the coverlay tape 30 can be removed easily with minimal damage to the substrate 100.

FIGs. 2a to 2h show a series of steps of a method for manufacturing semiconductor packages 200 according to the present invention, respectively.

A semiconductor package substrate 100 is provided, which includes a resin layer 6 and conductive circuit patterns. The resin layer 6 has a number of sub-strips 2, which constitute a main-strip 4 while slots 26 extend a predetermined length and act as boundaries among the sub-strips. Each sub-strip 2 has a number of through-holes 8 grouped in a number of rows and columns while being spaced a predetermined distance from one another, so that a semiconductor chip 42 can be positioned

thereon. The conductive circuit patterns include bond fingers 12 and ball lands 14 positioned on the resin layer 6 along the outer peripheral edge of the through-holes 8 of the sub-strips 2, so that the bond fingers 12 can be connected to semiconductor chips 42 by connection means 44 and conductive balls 48 can be melted and attached to the ball lands 14 in the following process. The surface of the resin layer 6 and the circuit patterns is coated with a cover coat 16 while exposing the bond fingers 12 and the ball lands 14 (refer to FIGs. 1a, 1b, and 2a).

Coverlay tape 24 is attached to a surface of each sub-strip 2 of the substrate 100 to close every through-hole 8 formed on the sub-strip 2 (FIG. 2b).

The coverlay tape has a cutting line 32 formed on the lower portion of the slot 26 at an interface between two sub-strips 2, to reduce the overall length of the coverlay tape. As a result, the difference in thermal expansion coefficient, which increases in proportion to the length, is reduced and warpage of the substrate 100 during processes for manufacturing semiconductor packages 200 is avoided.

Semiconductor chips 42 are positioned in the respective through-holes 8 of the substrate 100 with a surface thereof being attached to the coverlay tape 30 (FIG. 2c).

The semiconductor chips 42 are connected to the bond fingers 12 on the outer peripheral edge of the through-holes 8 with electrical connection means 44, such as gold wires or aluminum wires (FIG. 2d).

The through-holes 8 are molded with a sealant 46, such as an epoxy molding compound or a liquid sealant, to protect the semiconductor chips 42 and the connection means 44 from external environments (FIG. 2e).

Conductive balls 48, such as solder balls, are melted and attached to the ball lands 14 on the outer peripheral edge of the through-holes 8 (FIG. 2f).

The coverlay tape 30 is removed from the substrate 100 (FIG. 2g).

The coverlay tape 24 is removed by passing a punch 34 through the slot 26, which is formed at the interface between two sub-strips 2, to separate a side of the coverlay tape 30 from the substrate 100. In this manner, the coverlay tape 30 is easily removed from a surface of the sub-strips 2.

The outer peripheral edge of each through-hole 8 is cut in a singulation process to obtain separate semiconductor packages 200 (FIG. 3h).

Although a preferred embodiment of the present invention has been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions

and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

[EFFECT OF THE INVENTION]

The semiconductor package substrate and method for manufacturing semiconductor packages using the same according to the present invention are advantageous in that a cutting line is formed on the integral coverlay tape, which is attached to the substrate, to minimize warpage of the substrate resulting from the difference in thermal expansion coefficient, which increases in proportion to the length, and to prevent defects from occurring during processes for manufacturing semiconductor packages.

In addition, the coverlay tape can be easily removed from the substrate with minimal damage thereto by passing a punch through the slot, which is formed at the interface between two sub-strips, to separate an end of the coverlay tape during processes for manufacturing semiconductor packages.

(57) CLAIMS

1. A semiconductor package substrate comprising:

a resin layer having a number of sub-strips connected to one another to constitute a main-strip while slots extend a

predetermined length and act as boundaries among the sub-strips, each sub-strip having a number of through-holes grouped in predetermined rows and columns while being spaced a predetermined distance from one another so that a semiconductor chip can be positioned thereon;

a conductive circuit pattern having bond fingers and ball lands formed on a surface of the resin layer along an outer peripheral edge of the through-holes of the sub-strips so that semiconductor chips can be connected to the bond fingers by connection means and conductive balls can be melted and attached to the ball lands;

a cover coat formed on a surface of the resin layer and the circuit pattern while exposing the bond fingers and the ball lands; and

integral coverlay tape attached to a surface of the resin layer constituting the main strip to close the through-holes, the coverlay tape having a cutting line at an interface between two sub-strips.

2. The semiconductor package substrate as claimed in claim 1, wherein the cutting line of the coverlay tape spans an entire width of the coverlay tape.

3. The semiconductor package substrate as claimed in claim 1, wherein the cutting line of the coverlay tape spans a portion of an entire width of the coverlay tape including a region on the slot.

4. A method for manufacturing semiconductor packages comprising the steps of:

providing a semiconductor package substrate including a resin layer having a number of sub-strips connected to one another to constitute a main-strip while slots extend a predetermined length and act as boundaries among the sub-strips, each sub-strip having a number of through-holes grouped in predetermined rows and columns while being spaced a predetermined distance from one another so that a semiconductor chip can be positioned thereon, a conductive circuit pattern having bond fingers and ball lands formed on a surface of the resin layer along an outer peripheral edge of the through-holes of the sub-strips so that semiconductor chips can be connected to the bond fingers by connection means and conductive balls can be melted and attached to the ball lands, and a cover coat formed on a surface of the resin layer and the circuit pattern while exposing the bond fingers and the ball lands;

attaching integral coverlay tape to a surface of each sub-strip of the substrate to cover each through-hole of the sub-

strip, the coverlay tape having a cutting line at an interface between two sub-strips;

positioning semiconductor chips in the respective through-holes and attaching the semiconductor chips to the coverlay tape;

connecting the semiconductor chips to the bond fingers on the outer peripheral edge of the through-holes with electrical connection means;

filling the through-holes with a sealant to protect the semiconductor chips and the connection means from external environments;

removing the coverlay tape from the substrate;

melting and attaching conductive balls to the ball lands on the outer peripheral edge of the through-holes; and

cutting the outer peripheral edge of the through-holes to obtain separate semiconductor packages in a singulation process.

5. The method for manufacturing semiconductor packages as claimed in claim 4, wherein the cutting line of the coverlay tape spans an entire width of the coverlay tape.

6. The method for manufacturing semiconductor packages as claimed in claim 4, wherein the cutting line of the coverlay

tape spans a portion of an entire width of the coverlay tape including a region on the slot.

FIG.1a

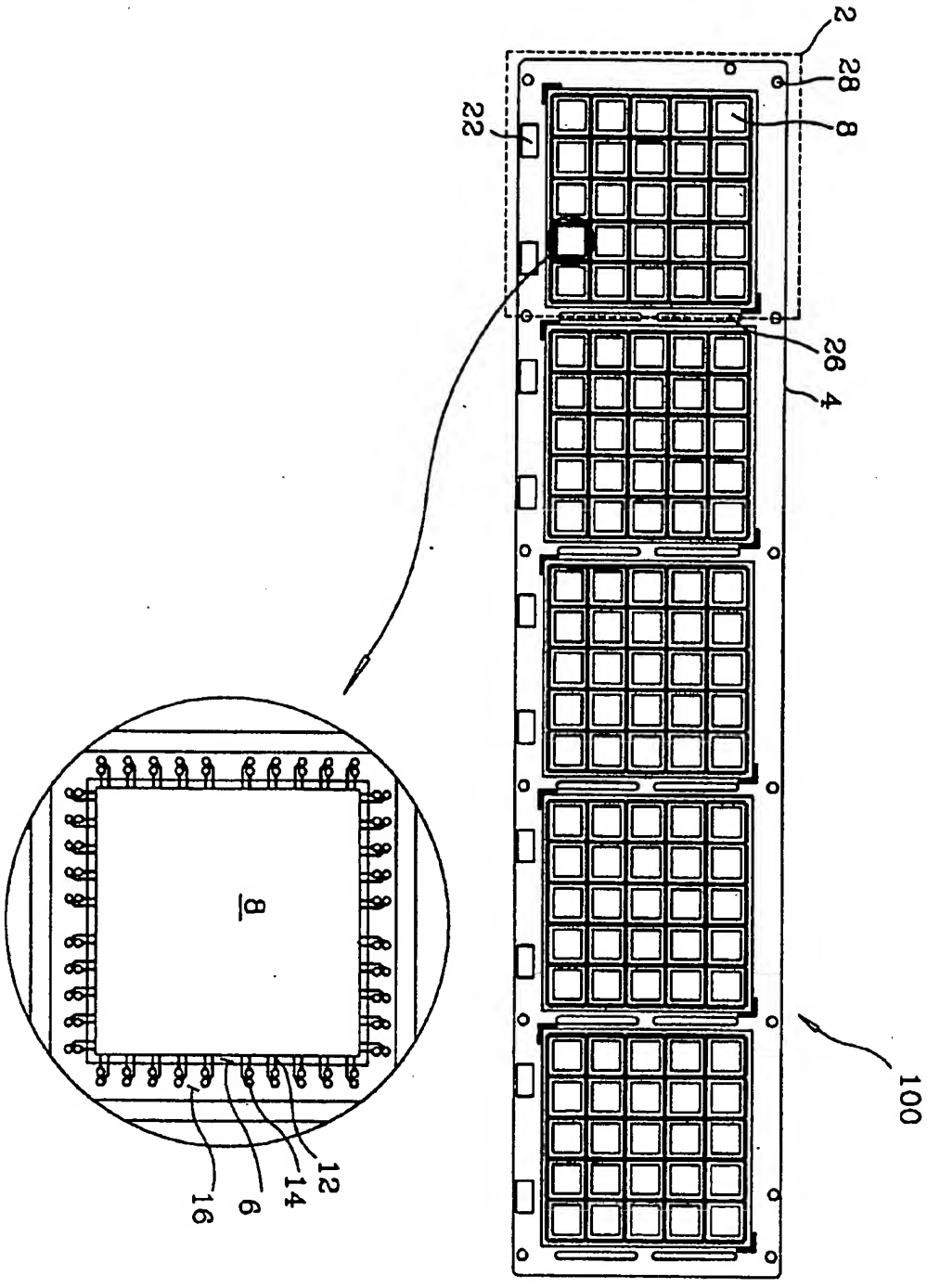

FIG.1b

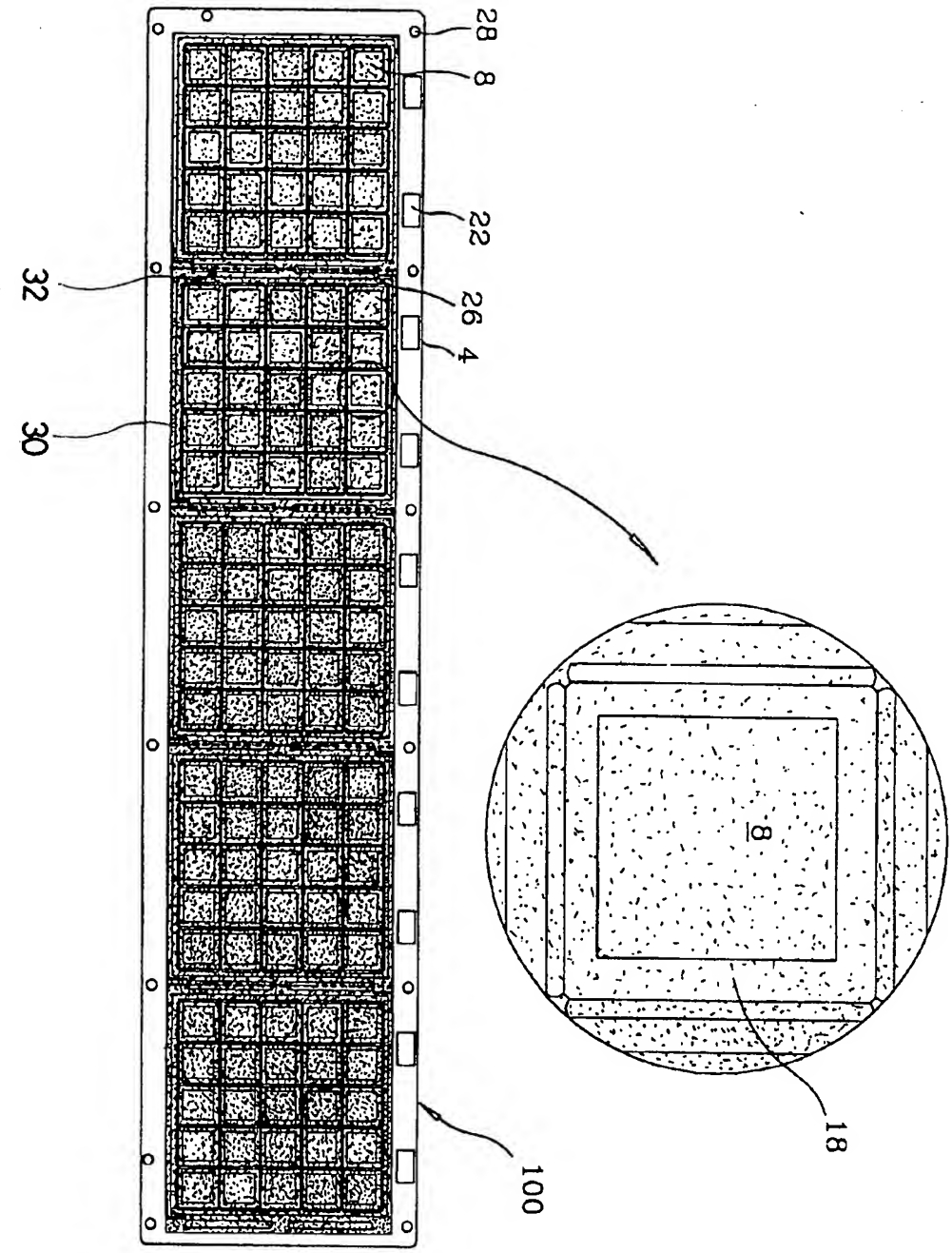

FIG.2a

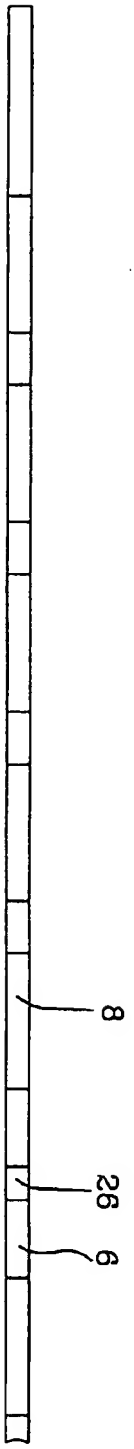
8
26
6

FIG.2b

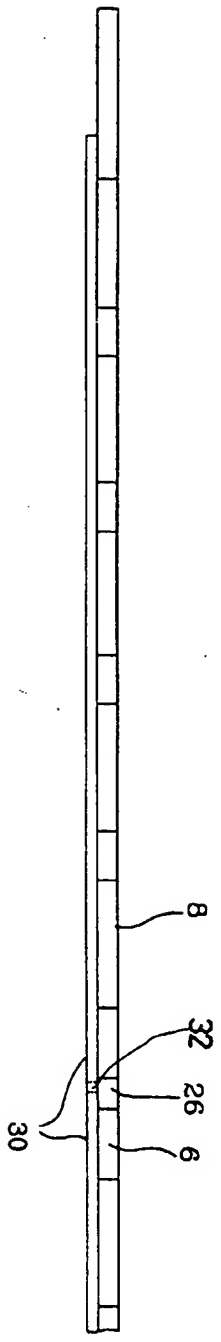

FIG.2c

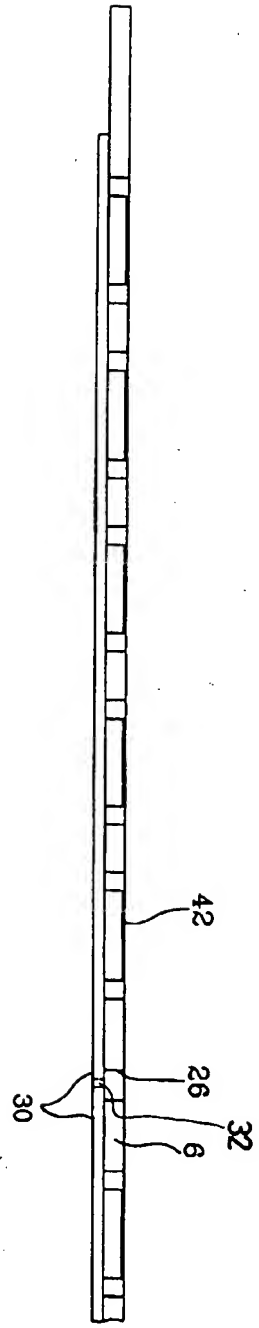

FIG.2d

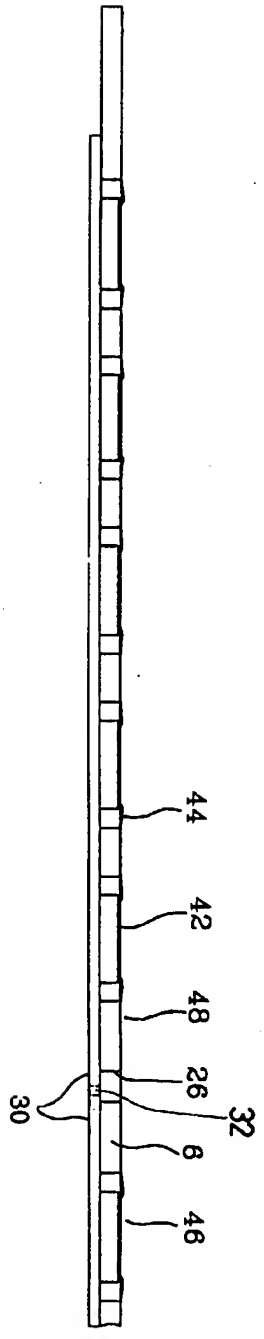

FIG.2e

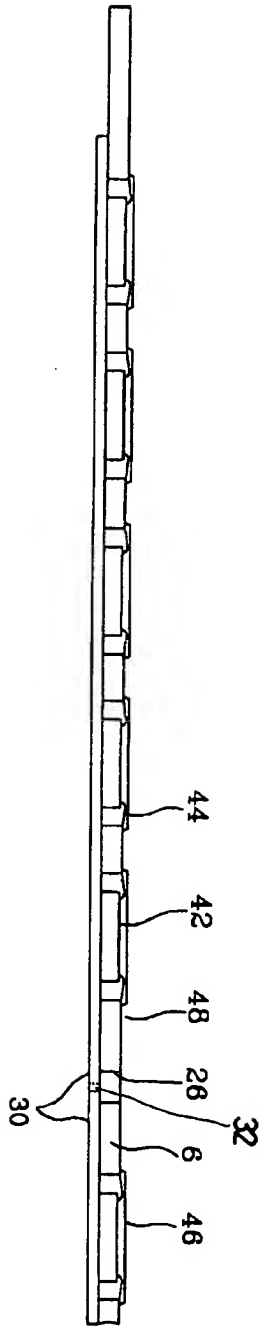

FIG.2f

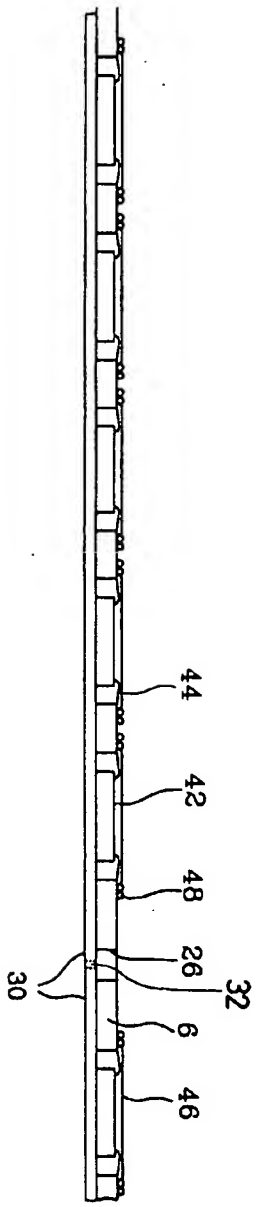

FIG.2g

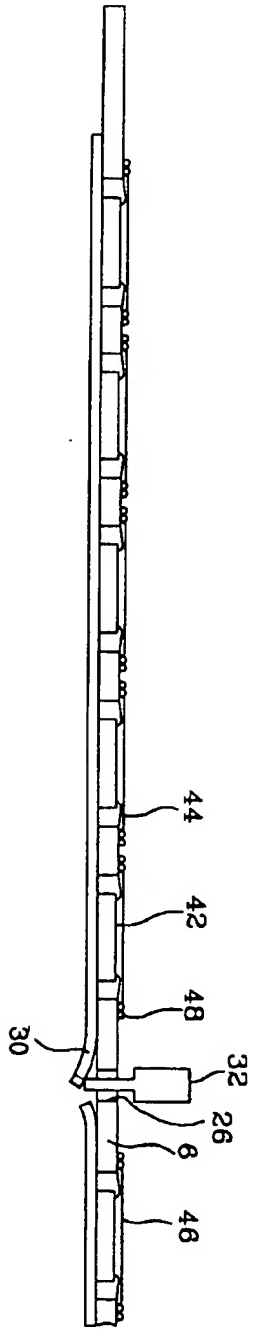

FIG.2h

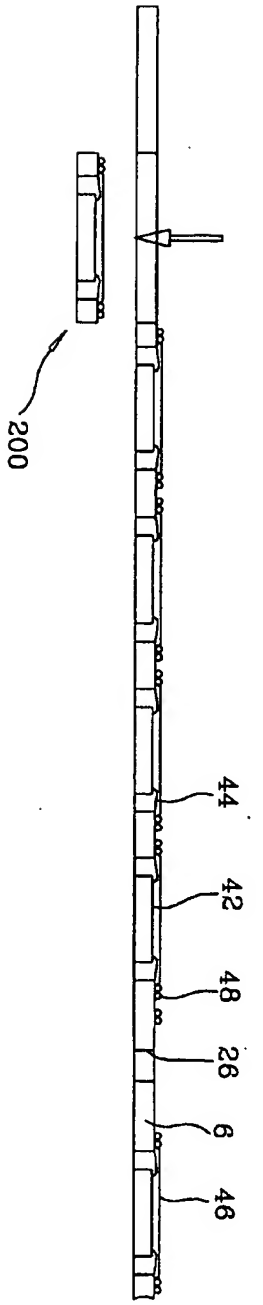

FIG.3